REMARKS

Claims 31-37 remain rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,937,424 of Leak et al. ("Leak") in view of Terada.

Applicants have amended the claims to more distinctly claim the invention. Applicants respectfully submit that the claims, as amended, are not rendered obvious by Leak in view of Terada.

Claim 31, as amended includes the following limitations

> A memory device, comprising:
>
> a memory array;
>
> a register to store at least one bit indicating a suspend status of a write operation for the memory array, and at least one bit indicating that a write operation was suspended due to an attempt to access data in a protected memory block; and
>
> a control circuit coupled to said memory array and said register, said control circuit to update said register and to control an output of a status signal representing said suspend status of said write operation, and wherein said control circuit includes:
>
> a first state machine to receive commands for accessing said memory array or said register, and
>
> a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

(Amended claim 31) (Emphasis added)

The Examiner has rejected claims 31-37 under 35 U.S.C. § 103(a) as being unpatentable over Leak in view of Terada. In particular, the Examiner has stated:

> The Leak *et al.* reference teaches a memory device which includes a memory array (understood), a register to store status information (see figure 7B, status register 142), a control circuit including a command decoder (first state machine) and a second state machine (see figure 7B, any of elements 190, 192, 194, 195, 196 and 198. The reference further teaches that it is advantageous to be able to suspend both erase and write (program) operations. The reference does not teach the particulars of the status register. The Terada reference has been discussed above. It teaches a status register that includes an "ESS" bit to indicate the erase suspend operation status. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modeled the Leak status register after the Terada status register to include an "ESS" bit to indicate that an erase operation has been suspended, and to further have modified the Terada status register to include a "WSS" bit to indicate that a write operation has been suspended. By the comparison to the prior art, it appears that Leak operates in byte write mode and that the byte write operation is suspended (claims 32 and 33). In keeping with the modification above, note that Terada teaches that if ESS=1, an erase operation is suspended, if ESS=0, then no erase is suspended. The modification suggested above would, by analogy, indicate that if WSS=1, then a write operation is suspended and if WSS=0, then no write operation is suspended (claim 32). The Leak command decoder has an input and clearly receives a status request signal to activate read status circuitry 198 (see figures 7A and 7B). The status register apparently outputs the status data on line RY/BY# (see figure 7B), presumably only ;upon request (claims 36 and 37).

(p.5-6 Office Action 6/21/01).

Applicants respectfully submit that neither Leak nor Terada, alone or in combination include the limitation of at least one bit indicating that a write

operation was suspended due to an attempt to access data in a protected memory block.

For this reason, applicants respectfully submit that amended claim 31 is not rendered obvious by Leak in view of Terada. Given that claims 32 – 37 depend, directly or indirectly, from claim 31, applicants respectfully submit that claims 32 – 37 are, likewise, not rendered obvious by Leak in view of Terada

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. Accordingly, applicants request that claims 31-37 be found in condition of allowance.

If there are any additional charges, please charge them to our Deposit Account No. 02-2666. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact Tom Van Zandt at (408) 720-8300.

Respectfully submitted,
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